

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. SP015.C17	APPLICATION NO. To Be Assigned
	APPLICANT Nguyen et al.	
	FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
/D.P./	AA1	3,346,851	10/1967	Thornton et al.			
	AB1	3,718,912	02/1973	Hasbrouck et al.			
	AC1	3,771,138	11/1973	Celtruda et al.			
	AD1	3,789,365	01/1974	Jen et al.			
	AE1	4,034,349	07/1977	Monaco et al.			
	AF1	4,200,927	04/1980	Hughes et al.			
	AG1	4,228,495	10/1980	Bernhard et al.			
	AH1	4,296,470	10/1981	Fairchild et al.			
	AI1	4,315,314	02/1982	Russo			
	AJ1	4,410,939	10/1983	Kawakami			
	AK1	4,434,461	02/1984	Puhl			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
/D.P./	AL1	0 479 390 A2	08/1992	EP			Yes No
	AM1	0 426 393	08/1991	EP			Yes No
	AN1	0 419 105 A2	10/1990	EP			Yes No
	AO1	0 402 856	12/1990	EP			Yes No
	AP1	0 377 991 A3	12/1989	EP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>1</u>	8-Bit Embedded controller Handbook, Intel, 1989, pp. 1-1- 1-19 and 3-1 -3-37.
/D.P./	AS	<u>1</u>	Acosta, Raymond D. et al., "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," IEEE Transactions on Computers, Vol. C-35, No. 9, September 1986, pp. 815-828.
/D.P./	AT	<u>1</u>	Agerwala et al., "High Performance Reduced Instruction Set Processors," IBM Research Division, March 31, 1987, pp. 1-61.

EXAMINER /Daniel Pan/	DATE CONSIDERED 07/08/2008
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
07/08/2008	AA2	4,459,657	07/1984	Murao			
	AB2	4,476,525	10/1984	Ishii			
	AC2	4,626,989	12/1986	Torii			
	AD2	4,675,806	06/1987	Uchida			
	AE2	4,714,994	12/1987	Oklobdzija et al.			
	AF2	4,722,049	01/1988	Lahti			
	AG2	4,752,873	06/1988	Shonai et al.			
	AH2	4,758,948	07/1988	May et al.			
	AI2	4,766,566	08/1988	Chuang			
	AJ2	4,807,115	02/1989	Torng			
	AK2	4,858,105	08/1989	Kuriyama et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
/D.P./	AL2	0 372 751 A2	11/1989	EP			Yes No
	AM2	0 368 332 A2	05/1990	EP			Yes No
	AN2	0 354 585 A2	02/1990	EP			Yes No
	AO2	0 171 595 A2	02/1986	EP			Yes No
	AP2	0 136 179 A2	09/1984	EP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>2</u>	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique*", pp. 221-235.
/D.P./	AS	<u>2</u>	Andrews, Distinctions Blur Between DSP Solutions, Computer Design, Vol. 28, No. 9, May 1, 1989, Littleton, Mass., pp. 86-99.
/D.P./	AT	<u>2</u>	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," Computer, Vol. 14, September 1981, pp. 18-27.

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/D.P./	AA3	4,897,810	01/1990	Nix			
↓	AB3	4,901,228	02/1990	Kodama			
	AC3	4,901,233	02/1990	Liptay			
	AD3	4,903,196	02/1990	Pomerene et al.			
	AE3	4,924,376	05/1990	Ooi			
	AF3	4,926,323	05/1990	Baror et al.			
	AG3	4,942,525	07/1990	Shintani et al.			
	AH3	4,985,825	01/1991	Webb, Jr. et al.			
	AI3	4,992,938	02/1991	Cocke et al.			
	AJ3	5,003,462	03/1991	Blaner et al.			
↓	AK3	5,101,341	03/1992	Circella et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
/D.P./	AL3	2 575 564	12/1985	FR			Yes No
↓	AM3	2 011 682	11/1979	GB			Yes No
	AN3	61-95447	06/1986	JP			Yes No
	AO3	2-278337	11/1990	JP			Yes No
↓	AP3	3-137729	06/1991	JP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>3</u>	Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler," Proceedings of the 2 nd International Conference on Architectural Support for Programming Languages and Operating Systems, October 1987, pp. 180-192.
/D.P./	AS	<u>3</u>	Foster et al., "Percolation of Code to Enhance Parallel Dispatching and Execution," IEEE Trans. On Computers, December 1971, pp. 1411-1415.
/D.P./	AT	<u>3</u>	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," ACM, 1988, pp. 442-452.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
/D.P./	AA4	5,127,091	02/1995	Horst			
↓	AB4	5,129,067	07/1992	Johnson			
	AC4	5,134,561	07/1992	Liptay			
	AD4	5,155,843	10/1992	Stamm et al.			
	AE4	5,187,796	02/1993	Wang et al.			
	AF4	5,226,126	07/1993	McFarland et al.			
	AG4	5,226,170	07/1993	Rubinfeld			
	AH4	5,230,068	07/1993	Van Dyke et al.			
	AI4	5,355,460	10/1994	Eickenmeyer et al.			
↓	AJ4	5,442,757	08/1995	McFarland et al.			
	AK4	5,461,715	10/1995	Matsuo et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
/D.P./	AL4	3-147134	06/1991	JP			Yes No
↓	AM4	2-22736	01/1990	JP			Yes No
	AN4	2-87229	03/1990	JP			Yes No
	AO4	3-35322	02/1991	JP			Yes No
↓	AP4	64-36366	02/1989	JP			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>4</u>	Gross et al., "Optimizing Delayed Branches," Proceedings of the 5 th Annual Workshop on Microprogramming, October 5-7, 1982, pp. 114-120.
/D.P./	AS	<u>4</u>	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," IEEE, 1989, pp. 134-137.
/D.P./	AT	<u>4</u>	Bakoglu et al., "IBM Second-Generation RISC Machine Organization," 1990, IEEE, pp. 173-178.

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/D.P./	AA5	5,487,156	01/1996	Popescu et al.			
	AB5	5,488,729	01/1996	Vesegna et al.			
	AC5	5,539,911	07/1996	Nguyen et al.			
	AD5	5,561,776	10/1996	Popescu et al.			
	AE5	5,574,927	11/1996	Scantlin			
	AF5	5,592,636	01/1997	Popescu et al.			
	AG5	5,625,837	04/1997	Popescu et al.			
	AH5	5,627,983	05/1997	Popescu et al.			
	AI5	5,651,125	07/1997	Witt et al.			
	AJ5	5,689,720	11/1997	Nguyen et al.			
	AK5	5,708,841	01/1998	Popescu et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
/D.P./	AL5	2-130634	05/1990	Japan			Yes No
	AM5						Yes No
	AN5						Yes No
	AO5						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>5</u>	H. Nakano et al., "A 80 Mflops 64-bit Microprocessor for Parallel Computer," 1991, IEEE, pp. 15.2.1-15.2.4.
/D.P./	AS	<u>5</u>	Hennessey et al., Computer Architecture: A Quantitative Approach, Morgan Kaufman Publishers, Inc., 1990 (in its entirety).
/D.P./	AT	<u>5</u>	Horst, R.W. et al., "Multiple Instruction Issue in the NonStop Cyclone Processor," IEEE, 1990, pp. 216-226.

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/D.P./	AA6	5,768,575	06/1998	McFarland et al.			
	AB6	5,778,210	07/1998	Henstrom et al.			
	AC6	5,797,025	08/1998	Popescu et al.			
	AD6	5,832,205	11/1998	Kelly et al.			
	AE6	5,832,293	11/1998	Popescu et al.			
	AF6	5,961,629	10/1999	Nguyen et al.			
	AG6	6,038,654	03/2000	Nguyen et al.			
	AH6	6,092,181	07/2000	Nguyen et al.			
	AI6	6,101,594	08/2000	Nguyen et al.			
	AJ6	6,128,723	10/2000	Nguyen et al.			
	AK6	5,233,694	08/1993	Hotta et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>6</u>	Hwu et al., "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," Proceedings from ISCA-13, Tokyo, Japan, June 2-5, 1986, pp. 297-306.
/D.P./	AS	<u>6</u>	Hwu et al., "Checkpoint Repair for High-Performance Out-of-Order Execution Machines," IEEE Trans. On Computers, Vol. C-36, NO. 12, December 1987, pp. 1496-1514.
/D.P./	AT	<u>6</u>	Hwu et al., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," Proceedings of the 15 th Annual Symposium on Computer Architecture, June 1988, pp. 45-53.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
	AB7						
	AC7						
	AD7						
	AE7						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL7						Yes No
	AM7						Yes No
	AN7						Yes No
	AO7						Yes No
	AP7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>7</u>	IBM Journal of Research and Development, Vol. 34, No. 1, January 1990, pp. 1-70.
/D.P./	AS	<u>7</u>	IBM Technical Disclosure Bulletin, Overlap of Store Multiple Operation With Succeeding Operations through Second Set of General Purpose Registers, Voll 28, No. 6, November 1989, New York, NY, pp. 2727-2728.
/D.P./	AT	<u>7</u>	Jelemensky, New Microcomputer Features Advanced Hardware For Real-Time Control Applications, Electro Conference Record, Vol. 14, April 11, 1989, Los Angeles, CA, pp. 511-519.

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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
	AB8						
	AC8						
	AD8						
	AE8						
	AF8						
	AG8						
	AH8						
	AI8						
	AJ8						
	AK8						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL8						Yes No
	AM8						Yes No
	AN8						Yes No
	AO8						Yes No
	AP8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>8</u>	Johnson, William M., Super-Scalar Processor Design, (Dissertation), copyright 1989, 134 pages.
/D.P./	AS	<u>8</u>	Johnson, William M., Super-Scalar Processor Design, Prentice-Hall, Inc., 1991 (in its entirety).
/D.P./	AT	<u>8</u>	Jouppi, N.H., "Integration and Packaging Plateaus of Processor Performance," IEEE, 1989, pp. 229-232.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
	AB9						
	AC9						
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	AK9						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL9						Yes No
	AM9						Yes No
	AN9						Yes No
	AO9						Yes No
	AP9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>2</u>	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," IEEE Transactions on Computers, Vol. 38, No. 12, December 1989, pp. 1645-1658.
/D.P./	AS	<u>9</u>	Jouppi et al., "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," Proceedings of the 3 rd International Conference on Architectural Support for Programming Languages and Operating Systems, April 1989, pp. 272-282.
/D.P./	AT	<u>2</u>	Keller, R.M., "Look-Ahead Processors," Computing Surveys, Vol. 7, No. 4, December 1975, pp. 177-195.

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	AA10						
	AB10						
	AC10						
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	AJ10						
	AK10						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL10						Yes No
	AM10						Yes No
	AN10						Yes No
	AO10						Yes No
	AP10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>10</u>	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," Annu. Rev. Comput. Sci., Vol. 4, 1990, pp. 173-201.
/D.P./	AS	<u>10</u>	Lee, Ruby B., "Precision Architecture," COMPUTER, January 1989, pp. 78-91.
/D.P./	AT	<u>10</u>	Melear, C., Motorola, Inc., The Design of the 88000 RISC Family, IEEE MICRO, Vol. 9, No. 2, April 1989, Los Alamitos, CA, pp. 26-38.

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	AA11						
	AB11						
	AC11						
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	AE11						
	AF11						
	AG11						
	AH11						
	AI11						
	AJ11						
	AK11						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL11						Yes No
	AM11						Yes No
	AN11						Yes No
	AO11						Yes No
	AP11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>11</u>	Murakami, K. et al., "SIMP (Single Instruction Stream/Multiple Instruction Pipelining): A Novel High-Speed Single-Processor Architecture," ACM, 1989, pp. 78-85.
/D.P./	AS	<u>11</u>	Odnert, D. et al., "Architecture and Compiler Enhancements for PA-RISC Workstations," Proceedings from IEEE Compcon, February 25-March 1, 1991, San Francisco, CA, pp. 214-218.
/D.P./	AT	<u>11</u>	Patent Abstracts of Japan, Vol. 010, No. 089, April 1986, & JP, A, 60 225 943 (Hitachi Seisakusho K K) November 11, 1985.

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	AA12						
	AB12						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL12						Yes No
	AM12						Yes No
	AN12						Yes No
	AO12						Yes No
	AP12						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>12</u>	Patt et al., "Critical Issues Regarding HPS, A High Performance Microarchitecture," Proceedings of the 18 th Annual Workshop on Microprogramming, December 1985, pp. 109-116.
/D.P./	AS	<u>12</u>	Patt et al., "HPS, A New Microarchitecture: Rationale and Introduction," Proceedings of the 18 th Annual Workshop on Microprogramming, December 1985, pp. 103-108.
/D.P./	AT	<u>12</u>	Pleszkun et al., "The Performance Potential of Multiple Functional Unit Processors," Proceedings of the 15 th Annual Symposium on Computer Architecture, June 1988, pp. 37-44.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA13						
	AB13						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL13						Yes No
	AM13						Yes No
	AN13						Yes No
	AO13						Yes No
	AP13						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>13</u>	Pleszkun et al., "WISQ: A Restartable Architecture Using Queues," Proceedings of the 14 th International Symposium on Computer Architecture, June 1987, pp. 290-299.
/D.P./	AS	<u>13</u>	Popescu et al., The Metaflow Architecture, Metaflow Technologies, Inc., June 1991(in its entirety).
/D.P./	AT	<u>13</u>	S. McGeady, "The i960A Superscalar Implementation of the 80960 Architecture," IEEE, 1990, pp. 232-240.

EXAMINER	/Daniel Pan/	DATE CONSIDERED	07/08/2008
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.P./

FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	ATTY. DOCKET NO. SP015.C17	APPLICATION NO. To Be Assigned
	APPLICANT Nguyen et al.	
	FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA14						
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL14						Yes No
	AM14						Yes No
	AN14						Yes No
	AO14						Yes No
	AP14						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>14</u>	Smith et al., Implementation Precise Interrupts in Pipelined Processors, IEEE Transactions on Computers, Vol. 37, No. 5, May 1988, New York, NY, p. 562, 573.
/D.P./	AS	<u>14</u>	Smith et al., "Implementation of Precise Interrupts in Pipelined Process," Proceedings of the 12 th Annual International Symposium on Computer Architecture, June 1985, pp. 36-44.
/D.P./	AT	<u>14</u>	Smith et al., "Limits on Multiple Instruction Issue," Proceedings of the 3 rd International Conference on Architectural Support for Programming Languages and Operating Systems, April 1989, pp. 290-302.

EXAMINER /Daniel Pan/	DATE CONSIDERED 07/08/2008
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL15						Yes No
	AM15						Yes No
	AN15						Yes No
	AO15						Yes No
	AP15						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>15</u>	Smith, M.D. et al., "Boosting Beyond Static Scheduling in a Superscalar Processor," IEEE, 1990, pp. 344-354.
/D.P./	AS	<u>15</u>	Sohi, Gurindar S. and Sriram Vajapeyam, "Instruction Issue Logic for High-Performance, Interruptable Pipelined Processors," Conference Proceedings of the 14 th Annual International Symposium on Computer Architecture, June 2-5, 1987, pp. 27-34.
/D.P./	AT	<u>15</u>	Thornton, J.E., Design of a Computer: The Control Data 6600, Control Data Corporation, 1970, pp. 58-140.

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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AM16						Yes No
	AN16						Yes No
	AO16						Yes No
	AP16						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>16</u>	Tjaden et al., "Detection and Parallel Execution of Independent Instructions," IEEE Trans. On Computers, Vol. C-19, No. 10, October 1970, pp. 889-895.
/D.P./	AS	<u>16</u>	Tjaden et al., "Representation of Concurrency with Ordering Matrices," IEEE Trans. On Computers, Vol. C-22, No. 8, August 1973, pp. 752-761.
/D.P./	AT	<u>16</u>	Tjaden, Representation and Detection of Concurrency Using Ordering Matrices, (Dissertation), 1972, pp. 1-199.

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	FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AM17						Yes No
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	AO17						Yes No
	AP17						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>17</u>	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," IBM Journal, Vol. 11, January 1967, pp. 25-33.
/D.P./	AS	<u>17</u>	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," Proceedings of the 19 th Annual Hawaii International Conference on System Sciences, 1986, pp. 41-50.
/D.P./	AT	<u>17</u>	Wedig, R.G., Detection of Concurrency in Directly Executed Language Instruction Streams, (Dissertation), June 1982, pp. 1-179.

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	APPLICANT Nguyen et al.	
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
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	AL18						Yes No
	AM18						Yes No
	AN18						Yes No
	AO18						Yes No
	AP18						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>18</u>	Weiss, R., Third-Generation RISC Processors, On Special Report, March 30, 1992, pp. 96-108.
/D.P./	AS	<u>18</u>	Weiss et al., "Instruction Issue Logic in Pipelined Supercomputers," Reprinted from IEEE Trans. On Computers, Vol. C-33, No. 11, November 1984, pp. 1013-1022.
/D.P./	AT	<u>18</u>	English Language Translation of Japanese Patent Appl. No. 61-95447, published May 14, 1986, 15 pages.

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	APPLICANT Nguyen et al.	
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL19						Yes No
	AM19						Yes No
	AN19						Yes No
	AO19						Yes No
	AP19						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>19</u>	English Language Translation of Japanese Patent Appl. No. 2-278337, published November 14, 1990, 20 pages.
/D.P./	AS	<u>19</u>	English Language Translation of Japanese Patent Appl. No. 3-137729, published June 12, 1991, 7 pages.
/D.P./	AT	<u>19</u>	English Language Translation of Japanese Patent Appl. No. 3-147134, published June 24, 1991, 18 pages.

EXAMINER /Daniel Pan/	DATE CONSIDERED 07/08/2008
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	APPLICANT Nguyen et al.	
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL20						Yes No
	AM20						Yes No
	AN20						Yes No
	AO20						Yes No
	AP20						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>20</u>	Kuga Morio et al., "Performance Evaluation of the Superscalar Processor "SIMP" based on the SIMP (Single Instruction Stream/Multiple Instruction Pipeline) Architecture," Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, 1990, pp. 337-344.
/D.P./	AS	<u>20</u>	English Language Translation, Kuga Morio et al., "Performance Evaluation of the Superscalar Processor "SIMP" based on the SIMP (Single Instruction Stream/Multiple Instruction Pipeline) Architecture," Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, 1990, pp. 337-344, (Document AR20).
/D.P./	AT	<u>20</u>	Kuga Morihiro et al., "Low-Level Parallel Processing Algorithm for the SIMP Processor Prototype," Department of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, Dec. 1989, pp. 1603-1611.

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	APPLICANT Nguyen et al.	
	FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
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	AM21						Yes No
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	AO21						Yes No
	AP21						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>21</u>	English Language Translation, Kuga Morihiro et al., "Low-Level Parallel Processing Algorithm for the SIMP Processor Prototype," Department of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, Dec. 1989, pp. 1603-1611, (Document AT20).
/D.P./	AS	<u>21</u>	US Application 09/336,589, Senter Cheryl et al., June 21, 1999.
/D.P./	AT	<u>21</u>	Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler," Proceedings of the 2 nd International Conference on Architectural Support for Programming Languages and Operating Systems, October 5-8, 1987, California.

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.	

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. SP015.C17	APPLICATION NO. To Be Assigned
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	FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AM22						Yes No
	AN22						Yes No
	AO22						Yes No
	AP22						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>22</u>	Notification of Reason for Refusal for Japanese Patent Application No. 2000-145123, mailed June 26, 2002, 2 pages.
/D.P./	AS	<u>22</u>	Notification of Reason for Refusal for Japanese Patent Application No. 2000-145124, mailed June 26, 2002, 2 pages.
/D.P./	AT	<u>22</u>	Notification of Reason for Refusal for Japanese Patent Application No. 2000-145125, mailed June 26, 2002, 2 pages.

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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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FOREIGN PATENT DOCUMENTS							
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	AO23						Yes No
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>23</u>	Notification of Reason for Refusal for Japanese Patent Application No. 2000-145126, mailed July 3, 2002, 2 pages.
/D.P./	AS	<u>23</u>	Notification of Reason for Refusal for Japanese Patent Application No. 2000-146442, mailed July 3, 2002, 2 pages.
/D.P./	AT	<u>23</u>	Notification of Reason for Refusal for Japanese Patent Application No. 2000-146443, mailed July 3, 2002, 2 pages.

EXAMINER	/Daniel Pan/	DATE CONSIDERED	07/08/2008
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	APPLICANT Nguyen et al.	
	FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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	AM24						Yes No
	AN24						Yes No
	AO24						Yes No
	AP24						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>24</u>	English-language translation of Japanese Laid-Open Patent Application No. H02-22736, (January 25, 1990 - date of publication), 10 pages.
/D.P./	AS	<u>24</u>	English-language translation of Japanese Laid-Open Patent Application No. H02-87229, (March 28, 1990 - date of publication), 5 pages.
/D.P./	AT	<u>24</u>	English-language translation of Notification of Reason for Refusal for Japanese Patent Application No. 2000-145123, mailed June 26, 2002, 3 pages.

EXAMINER	/Daniel Pan/	DATE CONSIDERED	07/08/2008
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	APPLICANT Nguyen et al.	
	FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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	AM25						Yes No
	AN25						Yes No
	AO25						Yes No
	AP25						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>25</u>	English-language translation for Notification of Refusal for Japanese Patent Application No. 2000-145124, mailed June 26, 2002, 3 pages.
/D.P./	AS	<u>25</u>	English-language translation for Notification of Refusal for Japanese Patent Application No. 2000-145125, mailed June 26, 2002, 4 pages.
/D.P./	AT	<u>25</u>	English-language translation for Notification of Refusal for Japanese Patent Application No. 2000-145126, mailed July 3, 2002, 3 pages.

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	APPLICANT Nguyen et al.	
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U.S. PATENT DOCUMENTS							
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	AM26						Yes No
	AN26						Yes No
	AO26						Yes No
	AP26						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>26</u>	English-language translation for Notification of Reason for Refusal for Japanese Patent Application No. 2000-146442, mailed July 3, 2002, 4 pages.
/D.P./	AS	<u>26</u>	English-language translation for Notification of Reason for Refusal for Japanese Patent Application No. 2000-146443, mailed July 3, 2002, 4 pages.
/D.P./	AT	<u>26</u>	Kuga Morihiro et al., "Low-Level Parallel Processing Algorithms for the "Shinpu" Processor Based on the SIMP (Single Instruction Stream / Multiple Instruction Pipelining) Method, Department of Information System, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, December 1989, pages 1603-1611.

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	FILING DATE Herewith	GROUP To be assigned

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
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	AM27						Yes No
	AN27						Yes No
	AO27						Yes No
	AP27						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
/D.P./	AR	<u>27</u>	English-language translation, Kuga Morihiro et al., "Low-Level Parallel Processing Algorithms for the "Shinpu" Processor Based on the SIMP (Single Instruction Stream / Multiple Instruction Pipelining) Method, Department of Information System, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, December 1989, pages 1603-1624.
/D.P./	AS	<u>27</u>	Final Rejection from Japanese Patent Appl. No. 502150, 1 page, (July 16, 2002)
/D.P./	AT	<u>27</u>	English translation of Final Rejection from Japanese Patent Appl. No. 502150, 1 page, (July 16, 2002)

EXAMINER /Daniel Pan/	DATE CONSIDERED 07/08/2008
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.P./

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT				ATTY. DOCKET NO. SP015.C17		APPLICATION NO. To Be Assigned	
				APPLICANT Nguyen et al.			
				FILING DATE Herewith		GROUP To be assigned	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
		AA28					
		AB28					
		AC28					
		AD28					
		AE28					
		AF28					
		AG28					
		AH28					
		AI28					
		AJ28					
		AK28					
FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
		AL28					Yes No
		AM28					Yes No
		AN28					Yes No
		AO28					Yes No
		AP28					Yes No
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
/D.P./	AR	<u>28</u>	English translation of Japanese Laid Open Patent Appl. No. H02-130634, (May 18, 1990 - date of publication), 56 pages.				
	AS	<u>28</u>					
	AT	<u>28</u>					
EXAMINER					DATE CONSIDERED		
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